µGPU : Embedded Digital ASIC GPU for Fabrication

SDMAY26-24

Colin McGann, Michael Drobot, Jack Tonn, Dawud Benedict,
Emil *Kosic, Josh Arceo, Sam Forde*
Client & Advisor: Dr. Henry John Duwe III

Introduction

- Modern GPUs are area and power hungry
- Identified 3 primary user groups
  - Embedded GPU Enthusiasts, Chip Forge members, & ISU faculty
- µGPU is an ASIC (Application Specific Integrated Circuit)
- Accelerates 3D graphics processing

Context

- µGPU must have a host machine to provide models & textures
- µGPU primarily used for raster graphics
- Software must be written in our custom ISA
- µGPU can be used for GPGPU operations
  - AI/ML, physics simulations

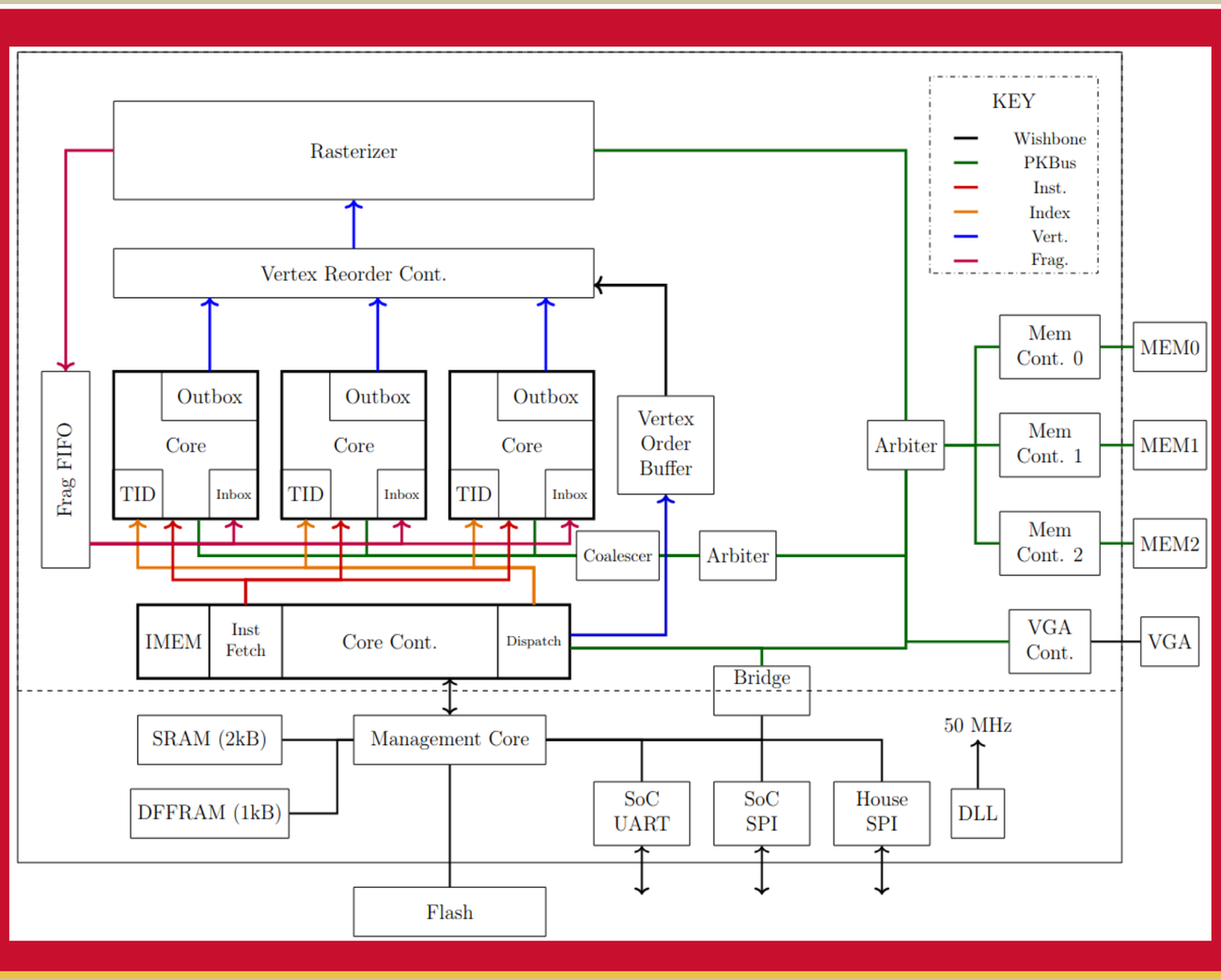
Design Requirements

Design Requirements
- Must fit in 10mm^2
- Output images at 320x240 resolution VGA
- Written in Verilog
- Maximum clock frequency of 50 MHz
- 8-bit color depth
- 38 GPIO pins

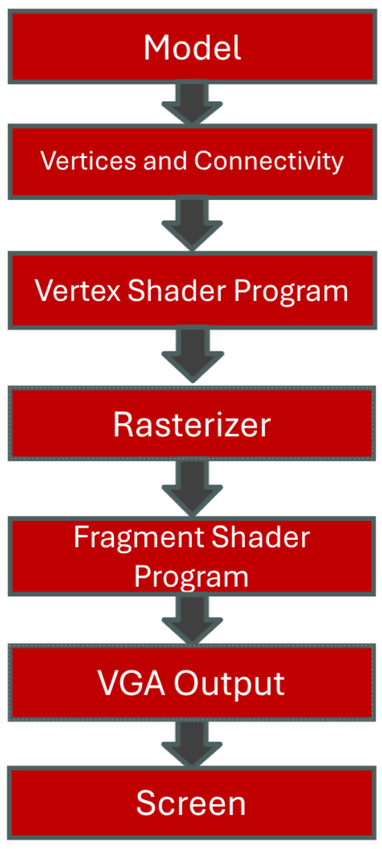
Design Approach

- Based on early programmable raster GPUs
- Build a system that can fit in the area
- Design a custom ISA for shader cores
- Modularize components for easier debugging

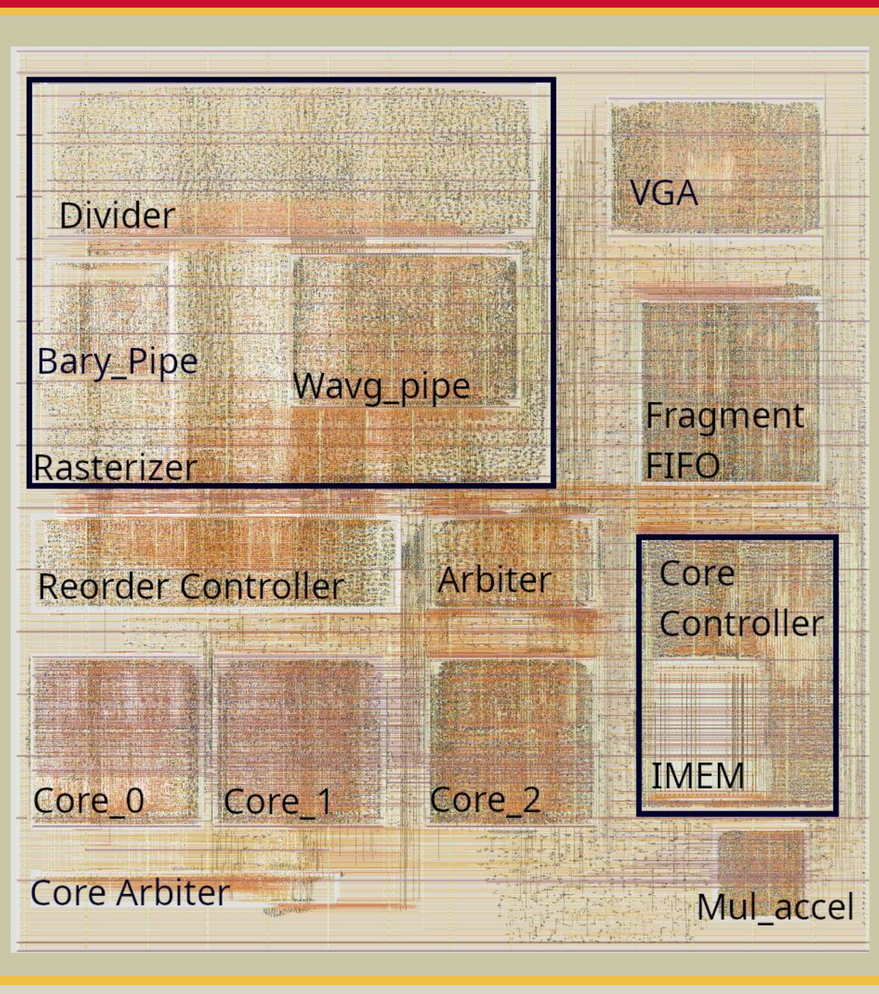
Technical Details



Dataflow



- Model vertices are loaded into memory with appropriate metadata
- Vertex shade is the process of converting 3D vertices to 2D screen space
- Rasterizer determines what triangles are shown where, and what texture each pixel is
- Fragment shade is the process of giving pixels color and writing to frame buffers



Area Table

Module	Dimensions (µm)	Area (mm^2)	Qty
Core	550x550	0.3025	3
VGA	700x450	0.36	1
Pre Rasterizer	1200x300	0.36	1
Rasterizer	1700x1300	2.21	1
Core Controller	650x900	0.585	1
Fragment FIFO	800x800	0.64	1
Cache	600x750	0.45	0
Wb_mul_accel	300x300	0.09	1
Core Arbiter	1000x100	0.1	1
Bridge	200x200	0.04	3
Bus Arbiter	450x450	0.2025	1
SPI Memory	300x300	0.09	3
Address Coalescer	850x850	0.7225	1
TOTAL USAGE		6.322 mm^2	63.22%

Note: Area table only shows the area of the hardened modules not consider the connections between them

Testing & Metrics

- Module level unit testing with SVUnit & Questasim
- Integration & system testing on Arty A7 FPGA
- Bringup plan provided to test individual hardware modules

Cube	Suzanne	Cow	Teapot	Chebureshka	Bunny
22.2 FPS	9.37 FPS	3.7 FPS	3.3 FPS	1.7 FPS	0.3 FPS

Conclusion

- Design is fully tested and working on FPGA
- Design has passed Chip Foundry precheck and will be taped out on May 13th, 2026
- Post-fabrication bringup will be done by returning members of senior design and ChipForge club members

https://sdmay26-24.sd.ece.iastate.edu/